CLAIMS

What is claimed is:

1. A method of making a semiconductor device comprising:

forming a semiconductor structure, the semiconductor structure including a top surface, a first sidewall, and a second sidewall opposing the first sidewall;

forming a first gate structure and a second gate structure, wherein the first gate structure is located adjacent to the first sidewall and the second gate structure is located adjacent to the second sidewall;

forming a third gate structure located over the top surface, wherein the first gate structure, the second gate structure, and the third gate structures are physically separate from each other.

2. The method of claim 1 wherein forming the first gate structure and the second gate structure further comprises depositing a layer of gate material over both the third gate structure and a substrate, and removing a portion of the layer of gate material overlying the third gate structure to form the first gate structure and the second gate structure.

3. The method of claim 2 wherein forming the first gate structure and the second gate structure further comprises non-abrasively etching the layer of gate material over the top surface of the semiconductor structure.

4. The method of claim 3 further comprising forming a substantially planar layer overlying the substrate below a height of a top surface of the layer of gate material and using the substantially planar layer as a masking layer to form the first gate structure and the second gate structure.

5. The method of claim 1 further comprising forming the third gate structure and the semiconductor structure by a single patterning step.

6. The method of claim 5 further comprises patterning a first dielectric material separating the semiconductor structure and the third gate structure and at least two additional layers overlying the third gate structure with the single patterning step.

7. The method of claim 1 further comprising:

forming a first source/drain region and a second source/drain region extending from the semiconductor structure on opposite sides of the semiconductor structure orthogonal to sides of the first gate structure and the second gate structure, wherein forming the first source/drain region and the second source/drain region further includes doping the integrated circuit at locations corresponding to the first source/drain region and the second source/drain region.

8. The method of claim 7 further comprising forming the first source/drain region and the second source/drain region by patterning the first gate structure, the second gate structure and the third gate structure to expose the first source/drain region and the second source drain region.

9. The method of claim 7 further comprising forming the first gate structure and the second gate structure subsequent to forming the first source/drain region and the second source/drain region by forming a substantially planar layer overlying the substrate below a height of a top surface of the layer of gate material and using the substantially planar layer as a masking layer to form the first gate structure and the second gate structure.

10. The method of claim 1 further comprising:

forming a first dielectric layer surrounding the first sidewall and the second sidewall of the semiconductor structure and electrically insulating the semiconductor structure from the first gate structure and the second gate structure; and

forming a second dielectric layer overlying the top surface of the semiconductor structure with a different processing step than used to form the first dielectric layer.

11. The method of claim 10 further comprising forming the first dielectric layer with a first dielectric material and forming the second dielectric layer with a second dielectric material, the second dielectric material comprising at least one physical property that differs from the first dielectric material.

12. The method of claim 11 further comprising selecting the at least one physical property from one of dielectric layer thickness, dielectric electrical conductivity or dielectric constant.

13. The method of claim 1 further comprising:

forming a charge storage structure, the charge storage structure located between the top surface and the third gate structure.

14. The method of claim 13 wherein the charge storage structure includes nanoclusters.

15. The method of claim 14 wherein the nanoclusters include at least one of silicon nanocrystals, germanium nanocrystals, silicon-germanium alloy nanocrystals, gold nanocrystals, silver nanocrystals, and platinum nanocrystals.

16. The method of claim 13 wherein the charge storage structure includes a charge trapping dielectric.

17. The method of claim 16 wherein the charge trapping dielectric includes at least one of silicon nitride, hafnium oxide, zirconium oxide, silicon rich oxide, and aluminum oxide.

18. The method of claim 1 further comprising:

forming a first charge storage structure located adjacent to the first sidewall, the first gate structure located adjacent to the first charge storage structure on an opposite side of the first charge storage structure from the first sidewall;

forming a second charge storage structure located adjacent to the second sidewall, the second gate structure located adjacent to the second charge storage structure on an opposite side of the second charge storage structure from the second sidewall.

19. The method of claim 18 further comprising:

forming a third charge storage structure, the third charge storage structure located between the top surface and the third gate structure.

20. The method of claim 1 further comprising:

forming electrical contacts only to two of the first gate structure, the second gate structure and the third gate structure.

21. The method of claim 1 further comprising:

forming electrical contact to only one of the first gate structure, the second gate structure and the third gate structure.

22. The method of claim 1 further comprising:

doping the third gate structure to have a resultant first conductivity type;

doping the first gate structure and the second gate structure to have a resultant second conductively type, the first conductively type being opposite the second conductivity type.

23. The method of claim 1 further comprising:

doping each of the first gate structure, the second gate structure and the third gate structure with differing conductivities.

24. The method of claim 1 wherein doping the first gate structure and the second gate structure further comprises angle implanting with different doping conditions.

25. A semiconductor device comprising:

a semiconductor structure including a top surface, a first sidewall, and a second sidewall opposing the first sidewall;

a first gate structure located adjacent to the first sidewall;

a second gate structure located adjacent to the second sidewall;

a third gate structure located over the top surface;

wherein first gate structure, the second gate structure and the third gate structures are physically separate from each other.

26. The semiconductor device of claim 25 further comprising:

a source region and a drain region extending from the semiconductor structure on opposite sides of the semiconductor structure orthogonal to sides of the first gate structure and the second gate structure;

wherein the first gate structure is located adjacent to the first sidewall at a location of the semiconductor structure between the source and the drain;

wherein the second gate structure is located adjacent to the second sidewall at a location of the semiconductor structure between the source and the drain; and

wherein the third gate structure is located over the top surface between the source and drain.

27. The semiconductor device of claim 25 further comprising:

a first dielectric layer surrounding the first sidewall and the second sidewall of the semiconductor structure and electrically insulating the semiconductor structure from the first gate structure and the second gate structure; and

a second dielectric layer overlying the top surface of the semiconductor structure, the first dielectric layer and the second dielectric layer comprising at least one differing physical property.

28. The semiconductor device of claim 27 wherein the at least one differing physical property comprising one of dielectric layer thickness, dielectric electrical conductivity or dielectric constant.

29. The semiconductor device of claim 25 further comprising:

a charge storage structure located between the top surface and the third gate structure.

30. The semiconductor device of claim 29 wherein the charge storage structure includes nanoclusters, wherein the nanoclusters include at least one of silicon nanocrystals, germanium nanocrystals, silicon-germanium alloy nanocrystals, gold nanocrystals, silver nanocrystals, and platinum nanocrystals.

31. The semiconductor device of claim 30 wherein the charge storage structure comprises a charge trapping dielectric.

32. The semiconductor device of claim 31 wherein the charge trapping dielectric comprises at least one of silicon nitride, hafnium oxide, zirconium oxide, silicon rich oxide, and aluminum oxide.

33. The semiconductor device of claim 25 further comprising:

a first charge storage structure located adjacent to the first sidewall, the first gate structure located adjacent to the first charge storage structure on an opposite side of the first charge storage structure from the first sidewall; and

a second charge storage structure located adjacent to the second sidewall, the second gate structure located adjacent to the second charge storage structure on an opposite side of the second charge storage structure from the second sidewall.

34. The semiconductor device of claim 33 wherein the first charge storage structure and the second charge storage structure include nanoclusters, wherein the nanoclusters comprise at least one of silicon nanocrystals, germanium nanocrystals, silicon-germanium alloy nanocrystals, gold nanocrystals, silver nanocrystals, and platinum nanocrystals.

35. The semiconductor device of claim 33 wherein the first charge storage structure and the second charge storage structure include a charge trapping dielectric wherein the charge trapping dielectric comprises at least one of silicon nitride, hafnium oxide, zirconium oxide, silicon rich oxide, and aluminum oxide.

36. The semiconductor device of claim 33 further comprising:

a third charge storage structure located between the top surface and the third gate structure, the third charge storage structure having at least one differing property from the first charge storage structure and the second charge storage structure.

37. The semiconductor device of claim 25 wherein:
the third gate structure is doped to have a first conductivity type; and
the first gate structure and the second gate structure are doped to have a second conductively type.

38. The semiconductor device of claim 25 wherein the first gate structure, the second gate structure and the third gate structure have differing conductivities.